Physical Layer controler LSI¡ÊPhy¡Ë

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¡¡MD8402¡¡¡¡¡¡200Mbps/3port¡¡¡¡3.3V¡¡¡¡100pLQFP¡¡¡¡Manufacturing

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The MD8402 is a controller for the high-speed serial bus physical layer that conforms to the IEEE 1394 - 1995. It can be connected to peripherals in a free configuration because it has the functions required for the physical layer and can control the three connected ports with a single chip. It has a direct interface with the link layer controller MD8412/13, so it is ideal for applications in which devices are built into peripherals or terminals.

BACK

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¡¡MD8405E¡¡ ¡¡ 400Mbps/3port¡¡¡¡3.3V¡¡¡¡80pLQFP¡¡¡¡Manufacturing

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The MD8405E is a controller for the high-speed serial bus physical layer that conforms to the IEEE 1394a-2000. It can be connected to peripherals in a free configuration because it has the functions required for the physical layer and can control the three connected ports with a single chip. It has a direct interface with the link layer controller MD8412/12B/15B/30, so it is ideal for applications in which devices are built into peripherals or terminals.

BACK

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¡¡MD8408B¡¡ ¡¡ 400Mbps/2port¡¡¡¡3.3V¡¡¡¡64pLQFP¡¡¡¡Manufacturing

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The MD8408B is a physical-layer IC intended to support the transfer speed of 400/200/100Mbit/sec., conforming to IEEE 1394a-2000. It offers two ports for the 1394-based cable interface, an interface for the link-layer IC, and the state machine logic for bus initialization and arbitration.

BACK

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Link Layer controler LSI ¡ÊLink¡Ë

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¡¡MD8412¡¡ ¡¡ 400Mbps¡¡¡¡5.0V¡¡¡¡100pLQFP¡¡¡¡Manufacturing

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The MD8412 is a link layer controller for high-speed serial buses, designed in accordance with the IEEE draft standard, IEEE 1394 - 1995. It involves all necessary functions for the link layer, and also functions to relieve the burden of the system for isochronous transfer. Therefore, it is suitable for being incorporated in equipment on the side of peripheral terminals.

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¡¡ Features

- Packing for transmission and unpacking for reception, according to IEEE 1394 - 1995
- Cycle master support
- Parity generation and error detection by 32-bit CRC
- Detection of dropped cycle start messages
- Support of both AC and DC coupling connections with PHY Interface
- 3-speed support of 100/200/400Mb/sec.
- Control of the No. of transfers in each cycle during isochronous transfer

- Automatic insertion of a header in isochronous packet during transmission and automatic header separation and routing during reception
- Support of outbound retry sequence
- Feasibility of selecting a host-bus width from 8/16/32-bit, enabling easy connection with a general-purpose MPU/microcomputer
- Support of both big and little-endians during selection of host bus 16/32-bit
- Support of control signals toward LPS (Link Power Status) of PHY (MD8402)

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Applications

[Digital camera] [Digital VTR] [Digital audio] [Electronic musical instruments] [Scanner] [Printer] [Various storages]

BACK

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¡¡**MD8412B**¡¡ ¡¡ 400Mbps¡¡¡¡3.3V¡¡¡¡100pLQFP¡¡¡¡Manufacturing

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The MD8412B is a link layer controller for high-speed serial buses, designed in accordance with the IEEE draft standard, IEEE 1394 -1995. It involves all necessary functions for the link layer, and also functions to relieve the burden of the system for isochro-nous transfer. Therefore, it is suitable for being incorporated in equipment on the side of peripheral terminals.

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¡¡ Features

- Packing for transmission and unpacking for reception, according to IEEE 1394-1995 and 1394a-2000
- Cycle master support
- Parity generation and error detection by 32-bit CRC
- Detection of dropped cycle start messages
- Direct with PHY chip (MD8402,MD8405E,MD8408B) and interface by AC coupling
- 3-speed support of 100/200/400Mb/sec.
- Control of the No. of transfers in each cycle during isochronous transfer
- Automatic insertion of a header in isochronous packet during transmission and automatic header separation and routingduring reception
- Support of outbound retry sequence
- Feasibility of selecting a host-bus width from 8/16/32-bit, enabling easy connection with a general-purpose MPU/micro-computer
- Support of both big and little-endians during selection of host bus 16/32-bit

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Applications

[Digital camera] [Digital VTR] [Digital audio] [Electronic musical instruments] [Scanner] [Printer] [Various storages]

BACK

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¡¡**MD8413**¡¡ ¡¡ 200Mbps¡¡¡¡3.3V¡¡¡¡100pLQFP¡¡¡¡Manufacturing

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The MD8413 is a controller for high-speed serial-bus link layers, arranged in accordance with IEEE 1394 -1995. It has all necessary functions for the link layer as a matter of course, and it also offers maximum transfer performance and variable system applications building with an isochronous transfer, by gaining access to the outside through an exclusive bus.

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Features

- Packing for transmission and unpacking for reception, according to IEEE 1394 - 1995
- Supporting the CycleMaster
- Parity generation and error detection by 32-bit CRC
- Detection of dropped cycle start messages
- Support of both AC and DC coupling connections with PHY Interface
- Controlling the transfer number for each cycle during isochronous transfer
- Automatic insertion of a header during transmission and automatic separation of the header during reception for the isochronous packet
- Full support of the out-bound retry sequence
- Data bus for exclusive isochronous send/receive
- Support of control signals toward LPS (Link Power Status) of PHY (MD8402)
- Supporting the bus time register

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Applications

[Digital camera] [Digital VTR] [Digital audio] [Electronic musical instruments(MIDI)] [Scanner] [Printer] [Various strorages] [DVD] [Set-top box] [Hardware 1394 Bus Analyzer]

BACK

¡¡**MD8415B**¡¡ ¡¡ 400Mbps¡¡¡¡3.3V¡¡¡¡144pLQFP¡¡¡¡Manufacturing

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The MD8415B is a link-layer controller of the high-speed serial bus, conforming to IEEE Standard 1394-1995. In addition to the various functions necessary for the link layer, the MD8415B is capable of supporting the register of the CSR space specified by IEEE 1394-1995. The asynchronous/isochronous packet offers maximum transfer performance by gaining access to the outside through an exclusive bus.

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Features

- Packing during transmission and unpacking during reception, conforming to IEEE1394-1995 and 1394a-2000.
- Supporting the CycleMaster.
- Supporting automatic activation of the Cycle Master.
- Parity generation by 32-bit CRC and error detection.
- Detection of a dropped cycle start message.
- Interface with the PHY chip (MD8402,MD8405E,MD8408B) supported by direct and AC coupling.
- Data bus exclusively provided for asynchronous transmission and reception.
- Controlling the number of transfer actions in each cycle during isochronous transfer.
- Automatic insertion of a header during isochronous packet transmission, and automatic separation of a header during reception.
- Full support of out-band retry sequence.
- Incorporating an exclusive data bus for isochronous transmission and reception, and an isochronous FIFO.
- Supporting a control signal toward the LPS Link Power Status) of the PHY (MD8402,MD8405E,MD8408B).
- Supporting the register of the CSR space specified by IEEE 1394-1995.

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Applications

[Digital camera] [Digital VTR] [Digital Audio] [Electronic Music Instrument] [Scanner] [Printer] [Each Storage] [DVD] [Set Top Box]

BACK

¡¡**MD8430**¡¡ ¡¡ 400Mbps¡¡¡¡3.3V¡¡¡¡128pLQFP¡¡¡¡Manufacturing

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The MD8430 is a link-layer controller of the high-speed serial bus, conforming to IEEE draft standard 1394-1995. The isochronous packet offers maximum transfer performance by gaining access to the outside through an exclusive bus. In addition to the various functions necessary for the link layer, the MD8430 is provided with the responder processing functions for the transaction layer. Therefore, it is capable of automatic transmission of a response packet for the request packet.

The internal register reads out the serial ROM for automatic setting. As a result, it is possible to make processing without any intervention of the host CPU in the case of applications that call for response transactions only.

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Features

- Packing during transmission and unpacking during reception, conforming to IEEE1394-1995.
- Cycle Master support.
- Parity generation by 32-bit CRC and error detection.
- Detection of a dropped cycle start message.
- DC and AC connections supported by the PHY-chip nterface.
- Controlling the number of transfer actions in each cycle during isochronous transfer.
- Automatic insertion of a header during isochronous packet transmission, and automatic separation of a header during reception.
- Full support of retry protocol.
- Exclusive data bus for isochronous transmission and reception.
- Supporting the bus time register.
- Enabling the connection with a PHY chip of 100, 200, or 400M/bps.
- Automatic transmission of a response packet in regard to the request packet.
- Automatic setting up of an internal register by the serial ROM.
- Function of SelfID packet analysis.
- DMA controller incorporated for send/receive data transfer, to be performed in conjunction with responder processing.
- Responder transactions processed without the host CPU.

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Applications

[Digital camera] [Printer] [Scanner] [Other devices to be controlled]

BACK